REMARKS

Claims 1-10, 12-14, and 26-29 are all the claims pending in the application. Claims 1-10 and 12-14 stand rejected on prior art grounds; and, claims 26-29 have been added. Claims Applicants respectfully traverse the rejections based on the following discussion.

I. The Prior Art Rejections

Claims 1, 6-8, and 13-14 stand rejected under 35 U.S.C. §102(b) as being anticipated by Pradeep (U.S. Patent No. 6,316,304), hereinafter referred to as "Pradeep". Claims 2-3 and 9-10 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Pradeep in view of Kao (U.S. Patent No. 6,500,765), hereinafter referred to as "Kao". Claims 4-5 and 12 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Pradeep in view of Ju (U.S. Patent No. 6,562,676), hereinafter referred to as "Ju". Applicants respectfully traverse these rejections based on the following discussion.

The claimed invention provides an integrated circuit structure comprising first-type transistors having first spacers and second-type transistors having first spacers, an etch stop layer, and second spacers. In the rejection, the Office Action argues that omitting the etch stop layer and second spacer from the first gate conductors would have been obvious. However, Pradeep clearly teaches that the etch stop layers and second spacers are formed over ***BOTH*** transistors – not selectively formed only over one of the transistors. Further, Applicants submit that it would not have been obvious to remove the etch stop layer only from the first transistor (or form an etch stop layer only on the second transistor) given the teachings of Kao because Kao fails to teach a device having an etch stop layer. Therefore, as explained in greater detail below, Applicants respectfully submit that the prior art of record does not teach or suggest the claimed invention.

The Office Action expressly acknowledges that Pradeep "fails to specify that the second spacers are only on said etch stop layer on said first spacers that are adjacent said second gate conductors, and said second spacers are not adjacent said first spacers that are adjacent said first gate conductors." Such features are defined in independent claim 26 using identical language. Furthermore, the Office Action admits that "Pradeep also fails to specify that the etch stop layer

is only on said first spacers that are adjacent said second gate conductors, and not on the first spacers of the first gate conductors." Such features are defined in independent claims 1, 8, and 26 using similar language. However, the Office Action argues that omitting the etch stop layer and second spacer from the first gate conductors would have been obvious given the teachings of Kao (Office Action, p. 4, para. 2).

Applicants respectfully disagree with such a conclusion. More specifically, the proposed combination of Pradeep and Kao would not have resulted in the claimed invention because nothing within Pradeep nor Kao teaches or suggests a method (or an apparatus produced thereby) of removing the etch stop layer and the second spacer from only the first transistor without removing the etch stop layer and the second spacer from the second transistor. Moreover, nothing within Pradeep nor Kao teaches or suggests a method (or an apparatus produced thereby) of forming the etch stop layer and the second spacer only on the second transistor without forming the etch stop layer and the second spacer on the first transistor.

Instead, Pradeep teaches forming the etch stop layers and second spacers simultaneously over ***BOTH TRANSISTORS***. As provided in column 3, lines 22-30 of Pradeep, an insulating liner layer 36 (which is proposed to be the first spacer in the Office Action) is deposited or grown overlying the gate structures 32/34 ***AND*** 32/35. Following this, an etch stop layer 38 is then deposited overlying the insulating liner layer 36. Moreover, as provided in column 3, lines 44-46 of Pradeep, a second spacer oxide layer 44 is deposited overlying the surface of ***BOTH*** transistor 46 and transistor 48.

Therefore, Pradeep clearly teaches that the etch stop layers and second spacers are formed over ***BOTH*** transistors – not selectively formed only over the second transistor. Moreover, nothing within Pradeep nor Kao teaches or suggests removing the etch stop layer and the second spacer from only the first transistor and maintaining the etch stop layer and the second spacer on the second transistor.

Further, Applicants submit that it would not have been obvious to remove the etch stop layer only from the first transistor (or form an etch stop layer only on the second transistor) given the teachings of Kao because Kao fails to teach a device having an etch stop layer. As illustrated in FIG. 5 of Kao, the device 110 comprises a dielectric layer 114a (which is proposed to be the

first spacer in the Office Action) and a first spacer 116b (which is proposed to be the second spacer in the Office Action). However, nothing within Kao illustrates or mentions etch stop layers. Thus, Kao cannot teach forming an etch stop layer only on the second transistor or removing an etch stop layer from only the first transistor.

In addition, Kao fails to disclose silicide regions proximate the spacers. Such a feature is defined in independent claims 1, 8, and 26 using the following language: "first silicide regions proximate said first spacers of said first-type transistors; and second silicide regions proximate said second spacers of said second-type transistors". There is only one mention of "silicide" within Kao, wherein the first gate 106a and the second gate 106b are formed from "metal silicide". However, with the exception of the gates, nothing within Kao mentions silicide regions. Therefore, Kao fails to teach or suggest silicide regions proximate the spacers (independent claims 1, 8, and 26).

Furthermore, Applicants respectfully submit that the obviousness rejection is technically defective because it does not provide a motivation to combine the prior art references. More specifically, the Office Action argues that Kao's teaching of larger spacers somehow would motivate one to omit the etch stop layer and the second spacer from slow diffuse transistors. However, the Office Action fails to provide any reasoning or explanation as to how such features would provide motivation to combine the teachings of Kao on the device of Pradeep. Applicants submit that there is no logical connection between using spacer thickness to control the diffusion rate of different FET devices and the removal of the etch stop layer and the second spacer.

Therefore, it is Applicants' position that the proposed combination of Kao and Pradeep does not teach or suggest many features defined by independent claims 1, 8, and 26 and that such claims are patentable over the prior art of record. Further, it is Applicants' position that dependent claims 2-7, 9-10, 12-14, and 27-29 are similarly patentable, not only because of their dependency from a patentable independent claims, but also because of the additional features of the invention they defined. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections.

II. Formal Matters and Conclusion

With respect to the rejections to the claims, the claims have been amended, above, to overcome these rejections. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections to the claims.

In view of the foregoing, Applicants submit that claims 1-10 and 12-14, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary. Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0458.

Respectfully submitted,

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